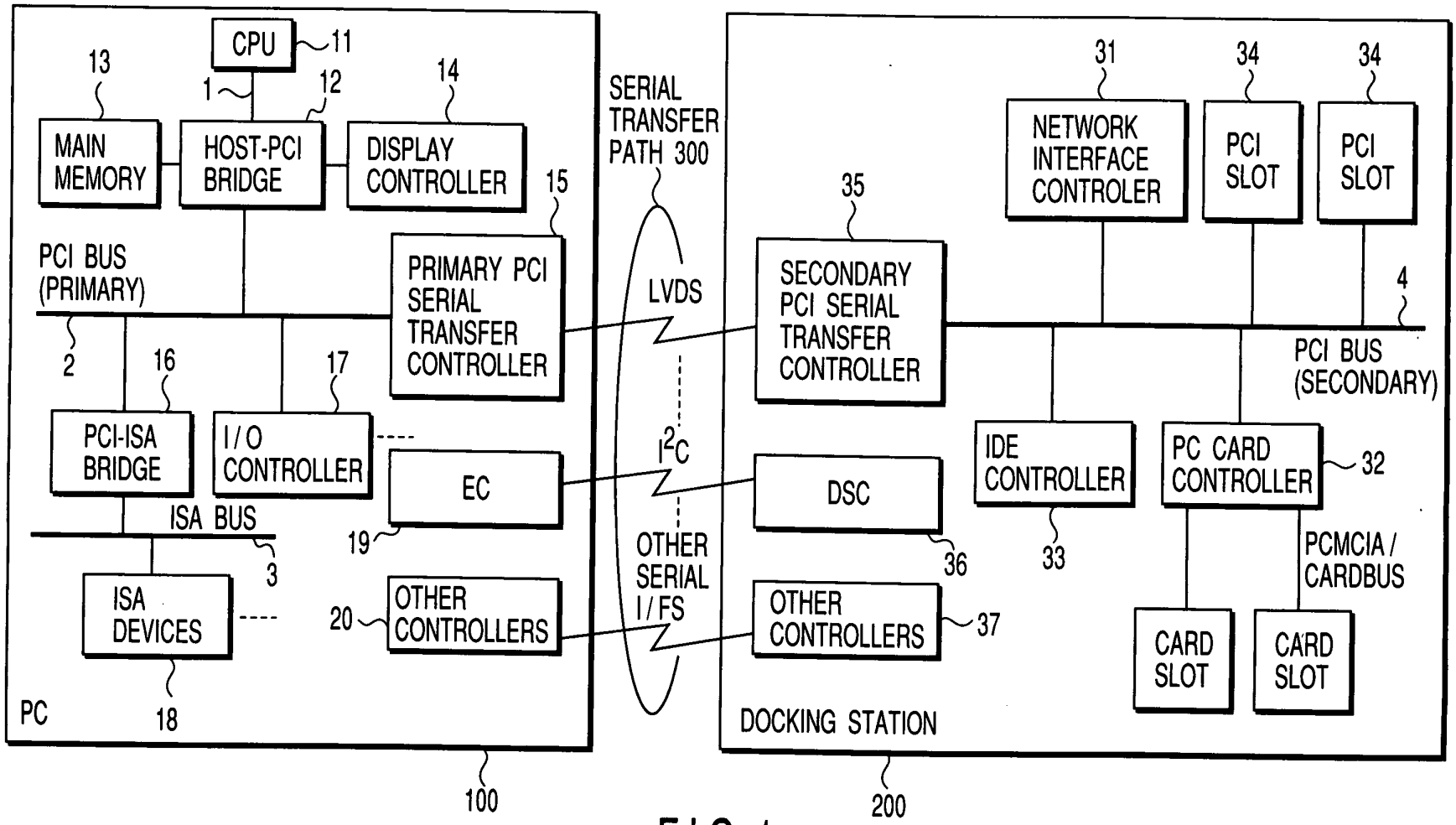

CPU
11
1
12
13
14
MAIN MEMORY
HOST-PCI BRIDGE
DISPLAY CONTROLLER
15
PCI BUS (PRIMARY)
PRIMARY PCI SERIAL TRANSFER CONTROLLER
2
16
17
PCI-ISA BRIDGE
I/O CONTROLLER
EC
ISA BUS
3
19
ISA DEVICES
18
20
OTHER CONTROLLERS
PC
100
SERIAL TRANSFER PATH 300
LVDS
I2C
OTHER SERIAL I/FS
31
34
34
NETWORK INTERFACE CONTROLER
PCI SLOT
PCI SLOT
35
SECONDARY PCI SERIAL TRANSFER CONTROLLER
4
PCI BUS (SECONDARY)
IDE CONTROLLER
PC CARD CONTROLLER
32
DSC
36
33
PCMCIA / CARDBUS
OTHER CONTROLLERS
37
CARD SLOT
CARD SLOT
DOCKING STATION
200

FIG. 1

DOCKET: 552260

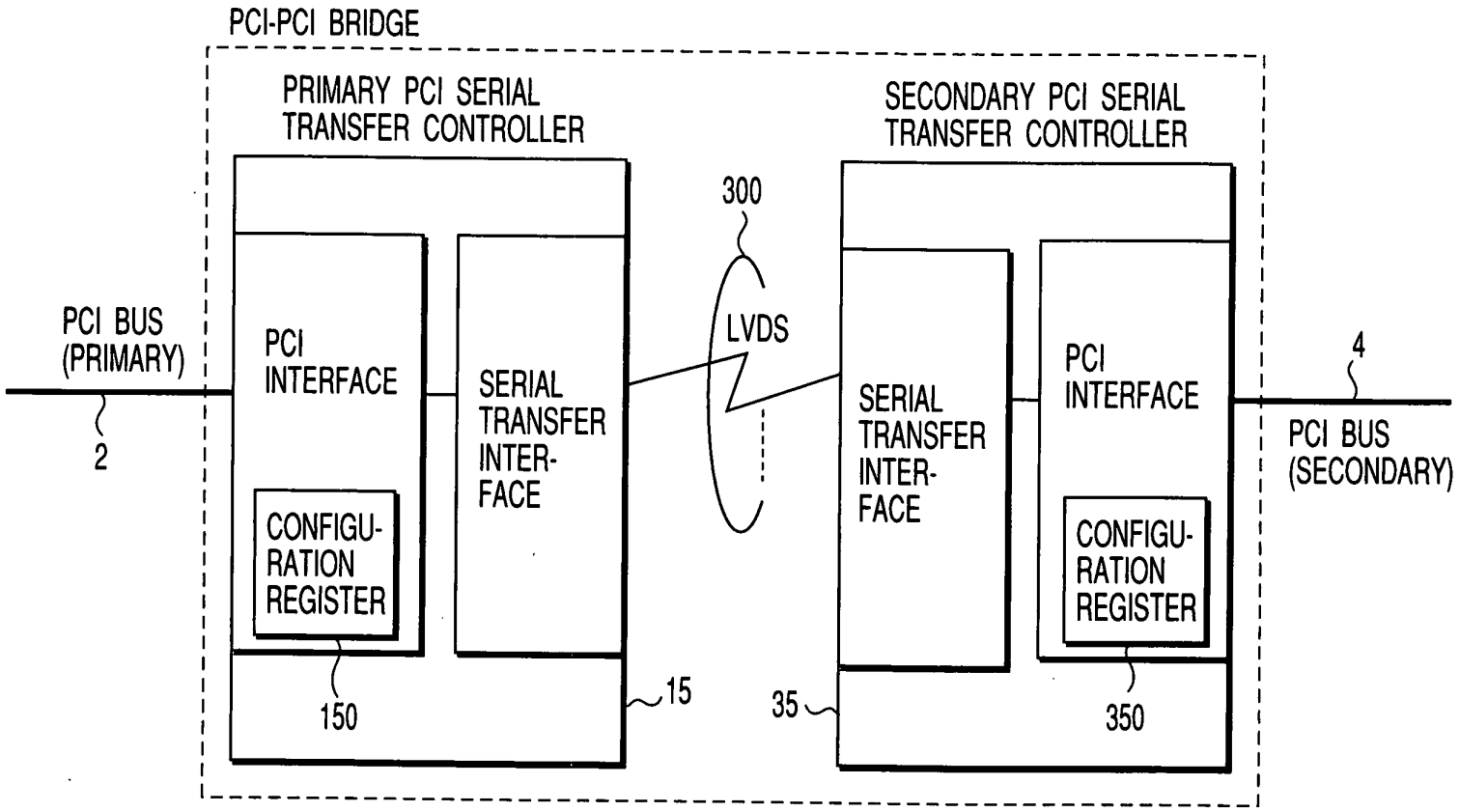


FIG. 2

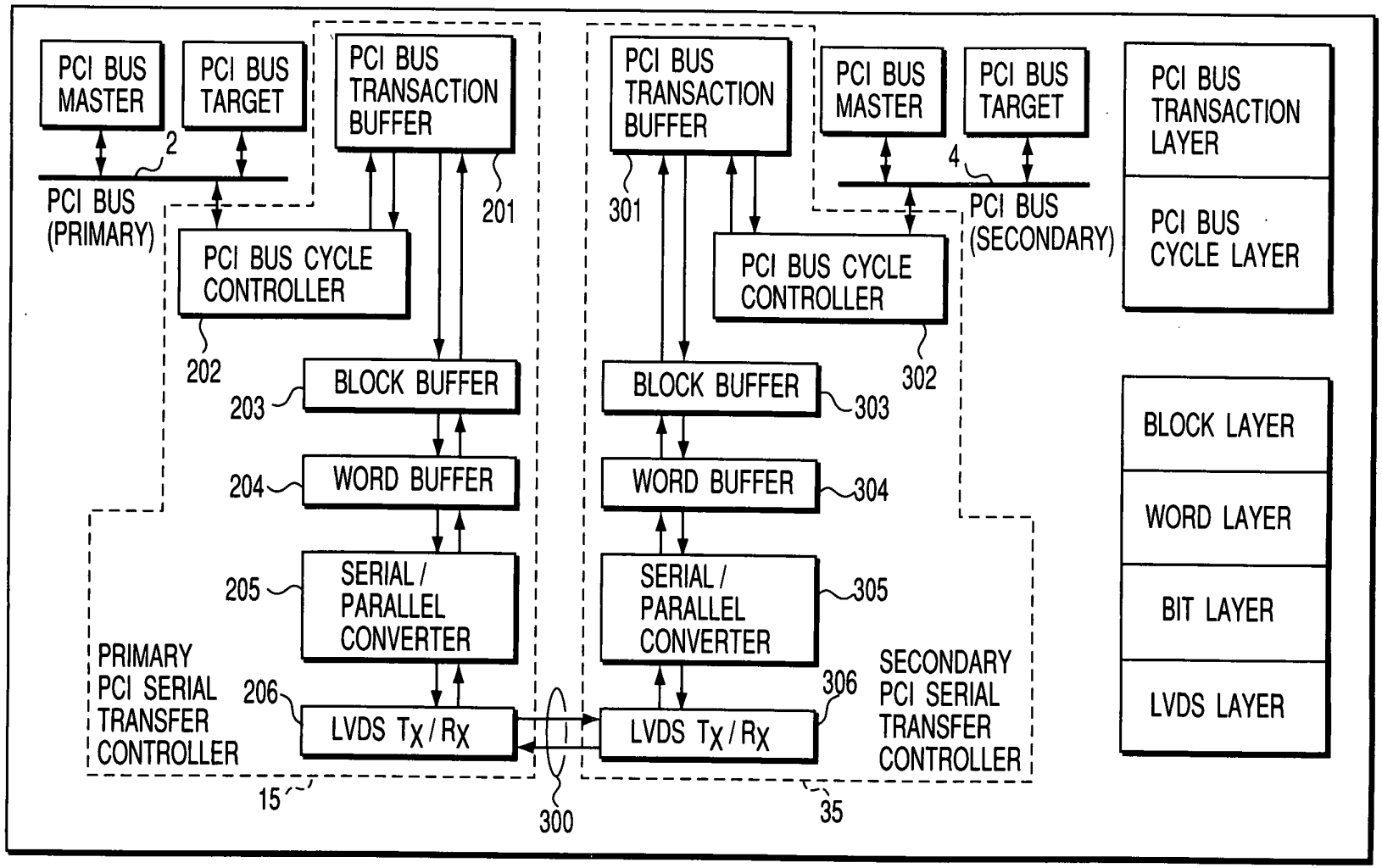

PCI BUS MASTER
PCI BUS TARGET
PCI BUS TRANSACTION BUFFER
2
PCI BUS (PRIMARY)
201
PCI BUS CYCLE CONTROLLER
202
BLOCK BUFFER
203
WORD BUFFER
204
SERIAL / PARALLEL CONVERTER
205
PRIMARY PCI SERIAL TRANSFER CONTROLLER
206
LVDS Tx / Rx
15
300
PCI BUS TRANSACTION BUFFER
301
PCI BUS MASTER
PCI BUS TARGET
4
PCI BUS (SECONDARY)
PCI BUS CYCLE CONTROLLER
302
BLOCK BUFFER
303
WORD BUFFER
304
SERIAL / PARALLEL CONVERTER
305
306
LVDS Tx / Rx
SECONDARY PCI SERIAL TRANSFER CONTROLLER
35
PCI BUS TRANSACTION LAYER
PCI BUS CYCLE LAYER
BLOCK LAYER
WORD LAYER
BIT LAYER
LVDS LAYER

FIG. 3

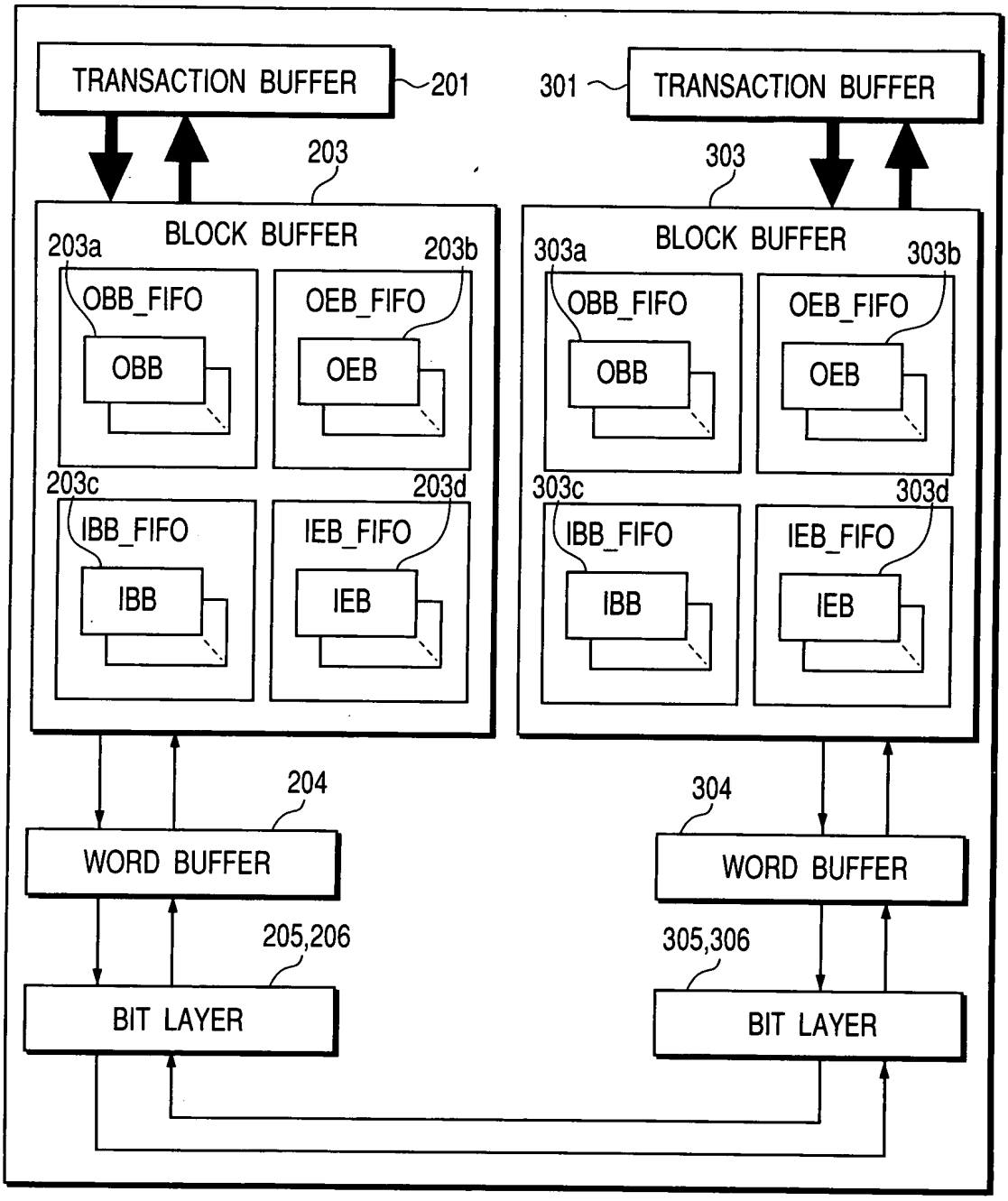

TRANSACTION BUFFER
201
301
TRANSACTION BUFFER
203
303
BLOCK BUFFER
203a
203b
OBB_FIFO
OEB_FIFO
OBB
OEB
BLOCK BUFFER
303a
303b
OBB_FIFO
OEB_FIFO
OBB
OEB
203c
203d
IBB_FIFO
IEB_FIFO
IBB
IEB
303c
303d
IBB_FIFO
IEB_FIFO
IBB
IEB
204
304
WORD BUFFER
WORD BUFFER
205,206
305,306
BIT LAYER
BIT LAYER

FIG. 4

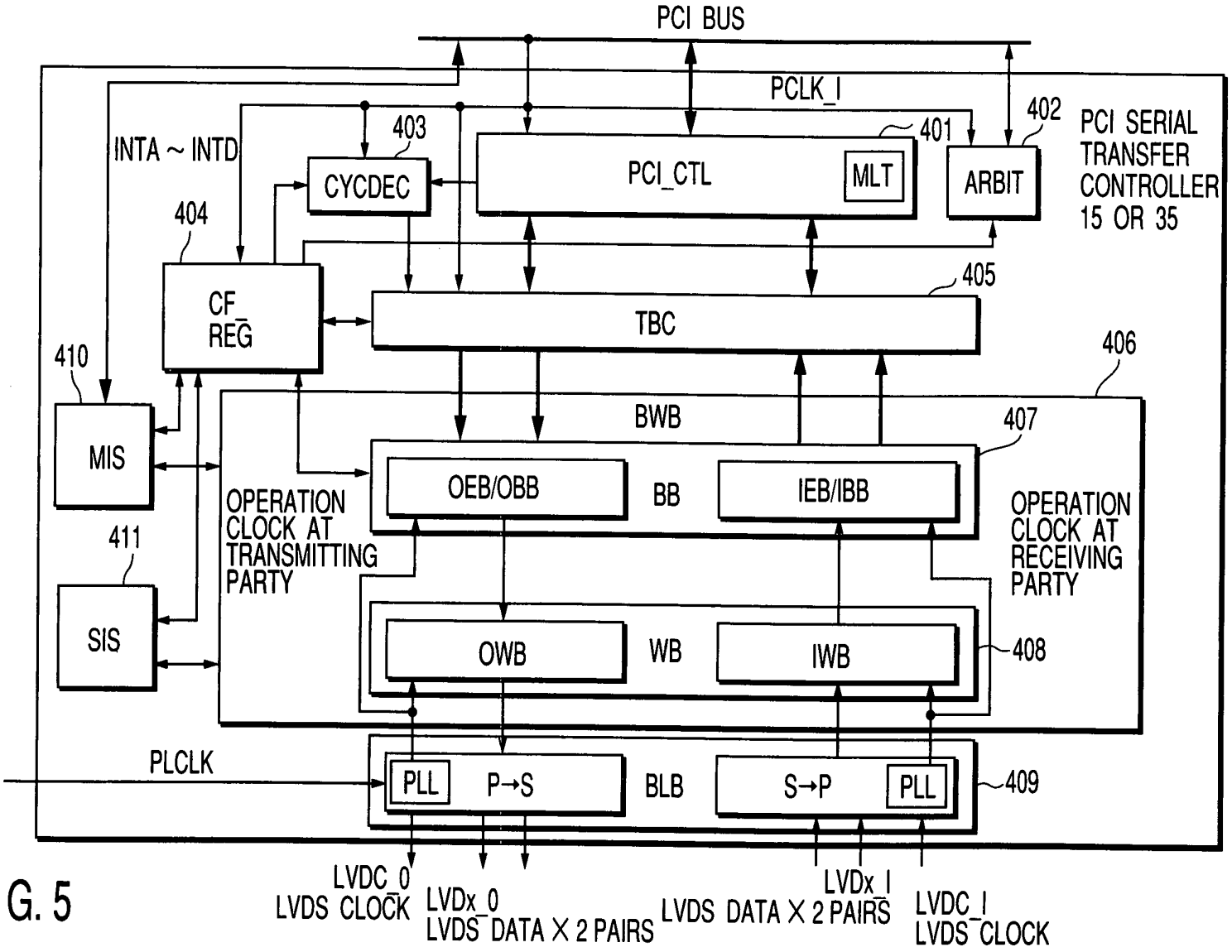
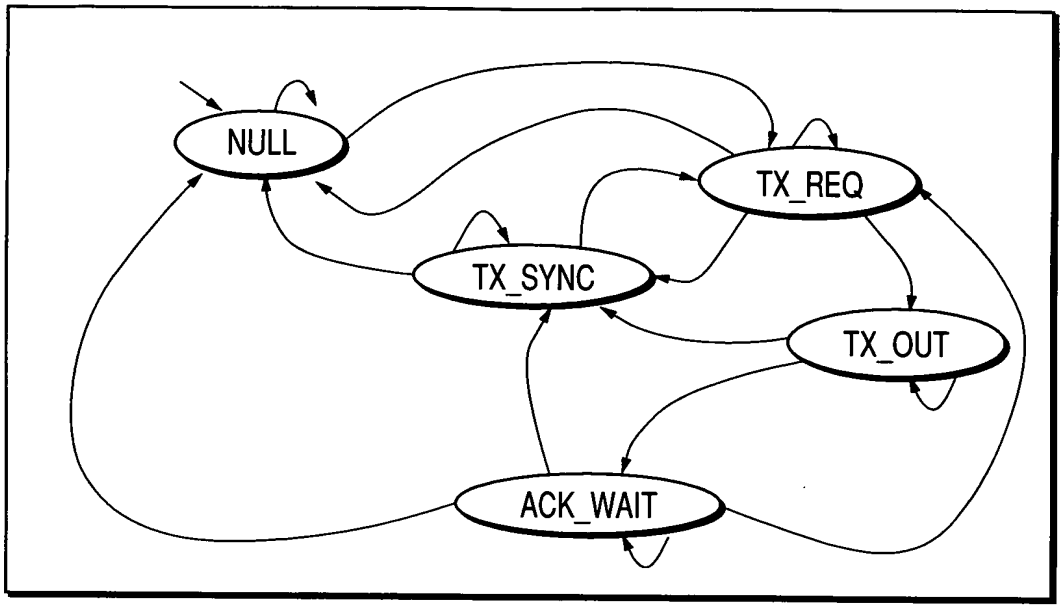

PCI BUS
PCLK_I
INTA ~ INTD
403
401
402
PCI SERIAL TRANSFER CONTROLLER 15 OR 35
CYCDEC
PCI_CTL
MLT
ARBIT
404
405
CF_REG
TBC
406
410
BWB
407
MIS
OEB/OBB
BB
IEB/IBB
OPERATION CLOCK AT TRANSMITTING PARTY
OPERATION CLOCK AT RECEIVING PARTY
411
SIS
OWB
WB
IWB
408
PLCLK
PLL
P→S
BLB
S→P
PLL
409
LVDC_0
LVDS CLOCK
LVDx_0
LVDS DATA X 2 PAIRS
LVDx_1
LVDS DATA X 2 PAIRS
LVDC_1
LVDS CLOCK

FIG. 5



OBB STATE TRANSITION

FIG. 6

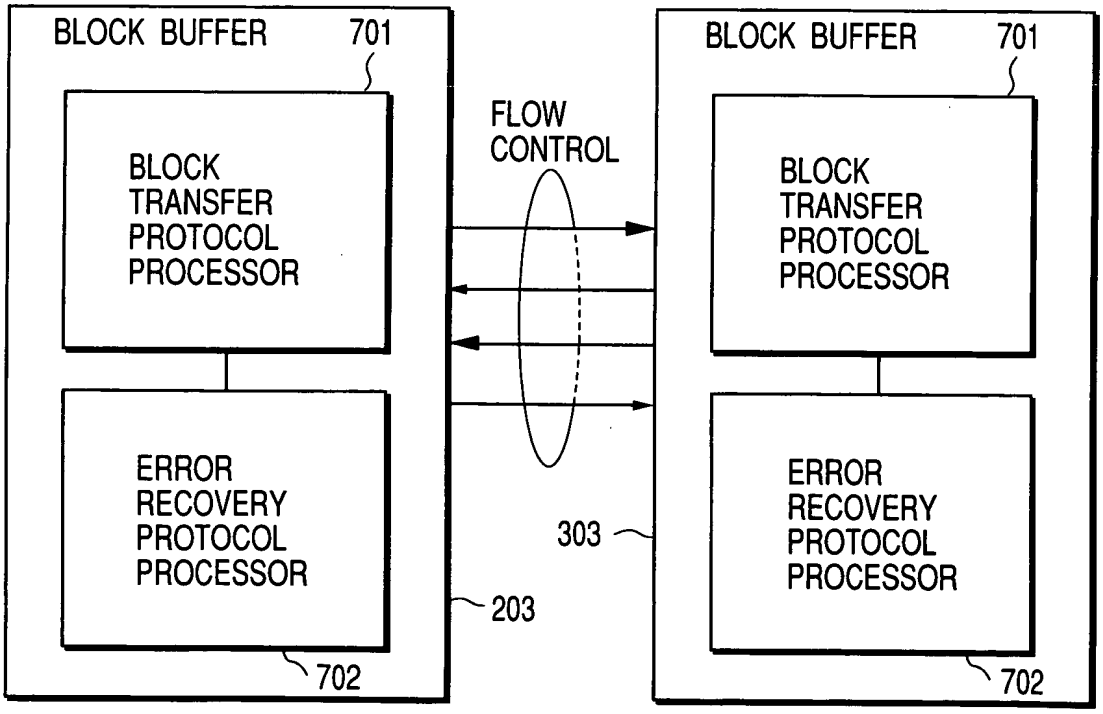


FIG. 7

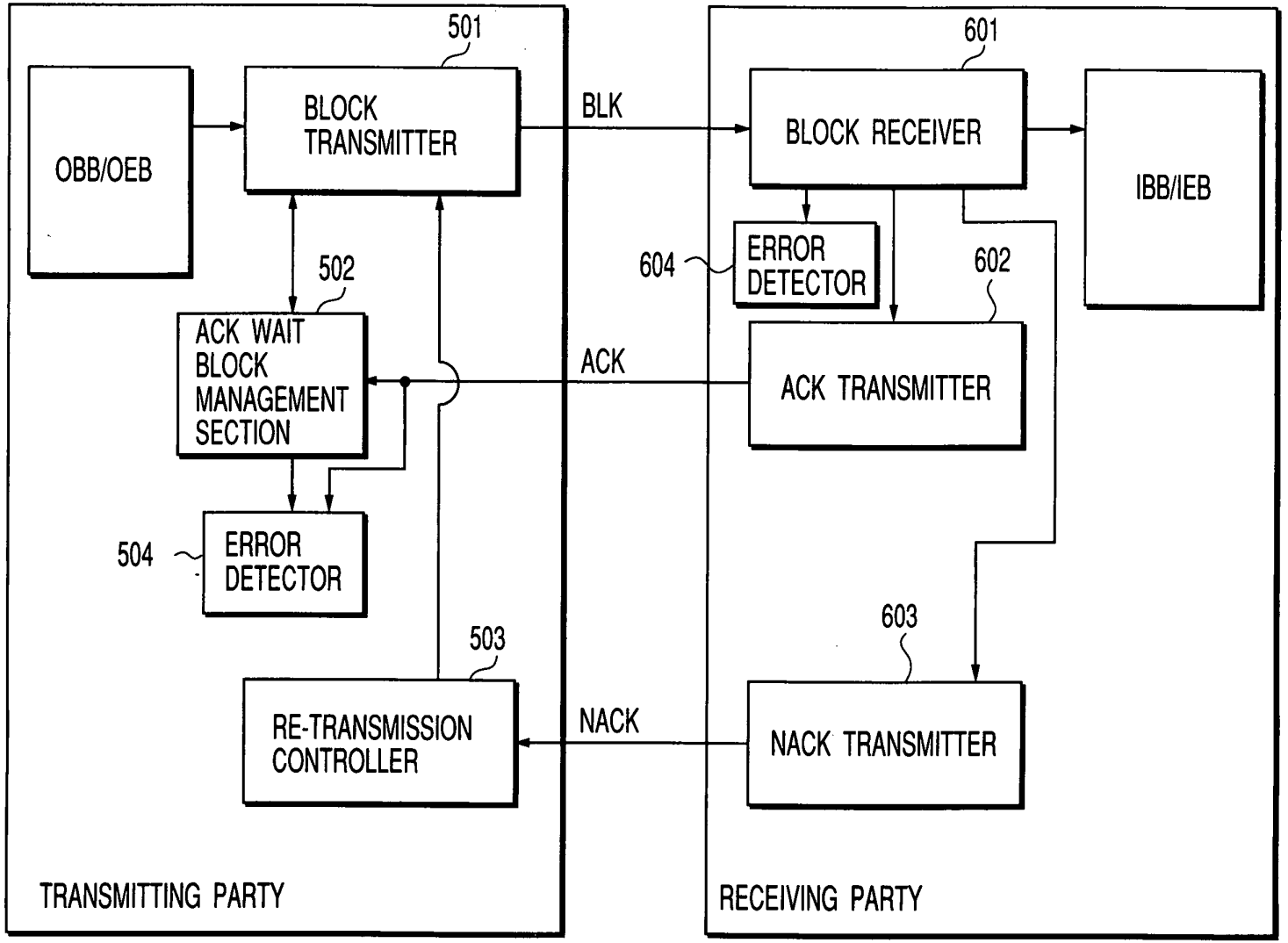
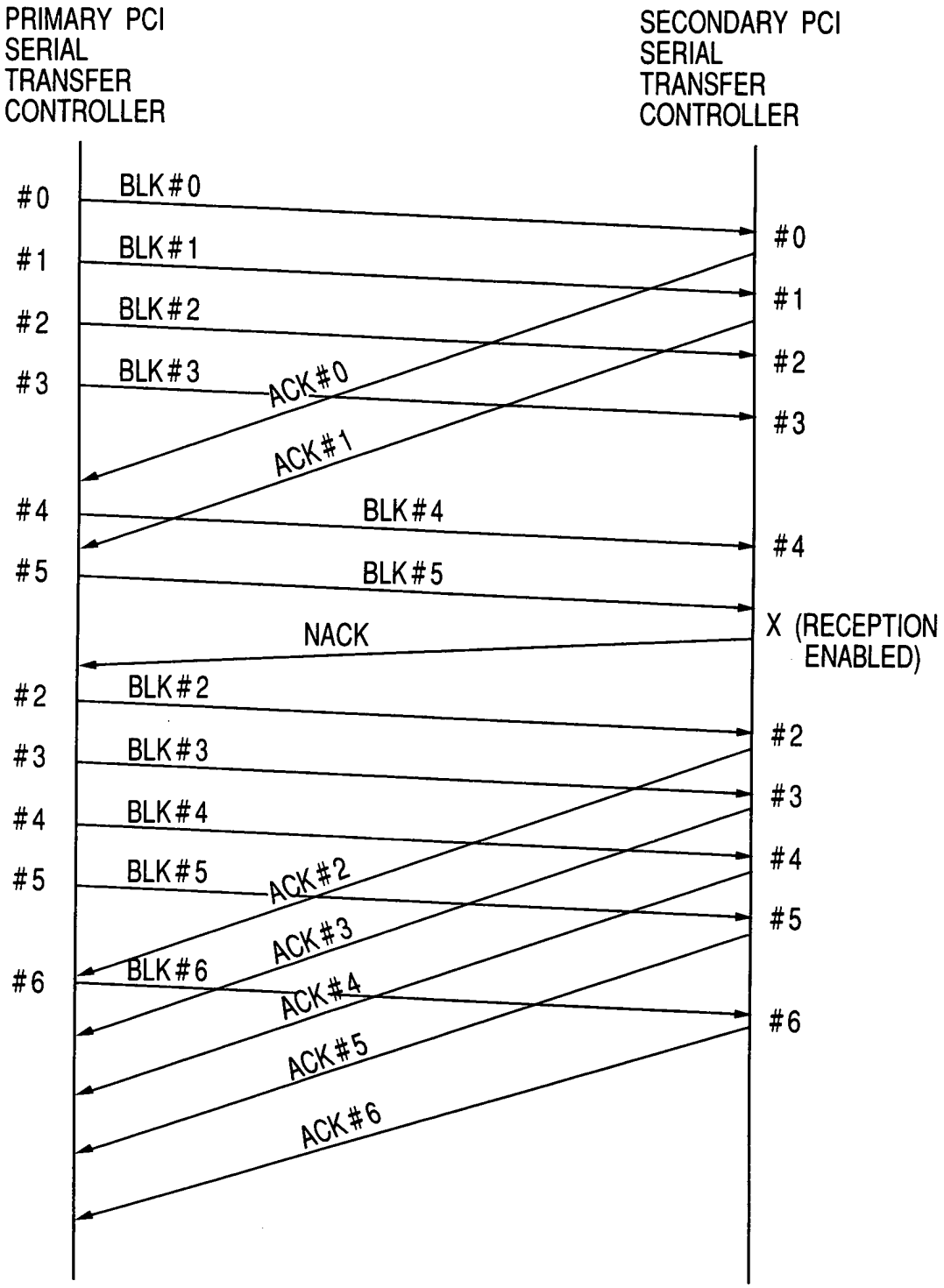
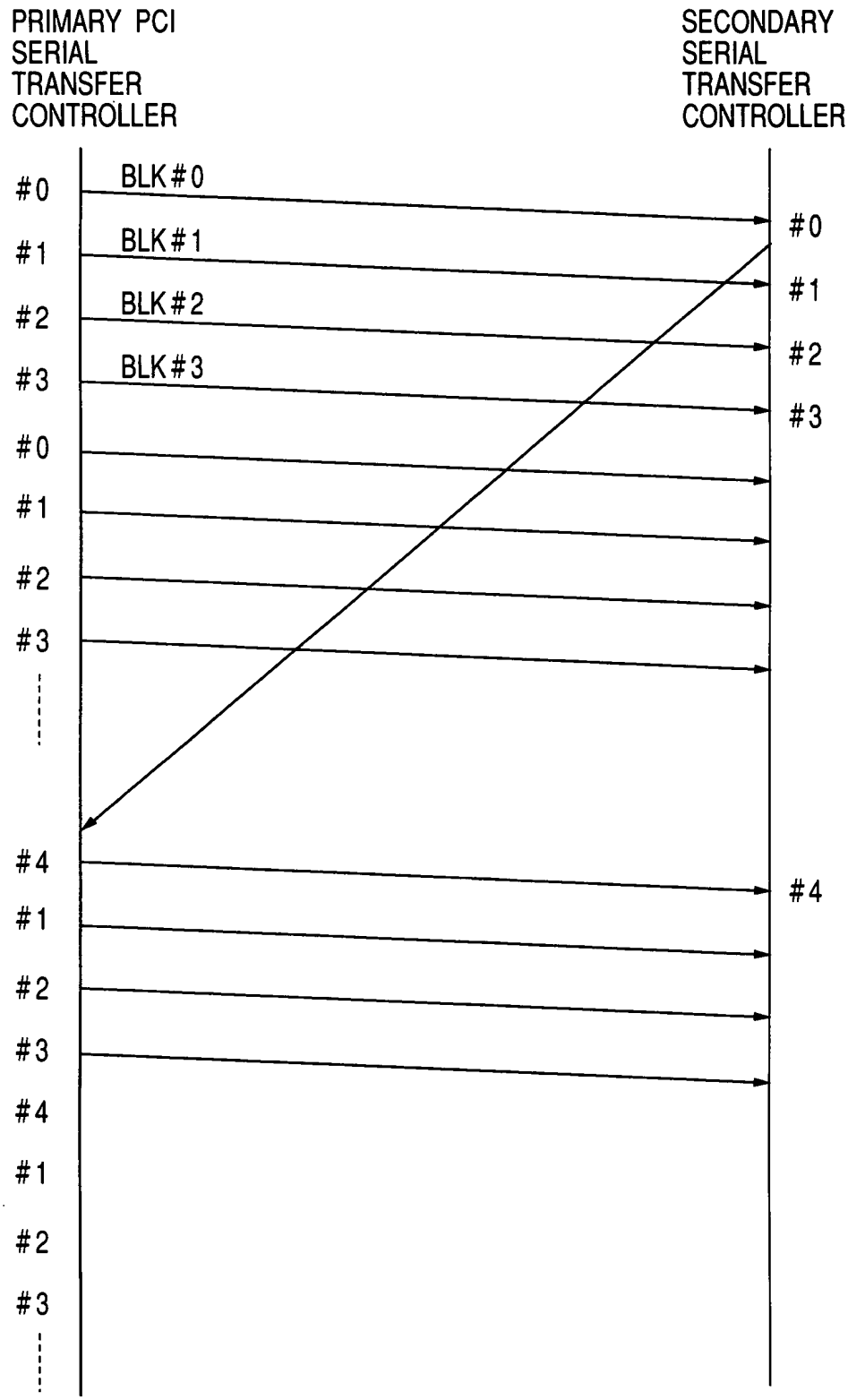

501
601
OBB/OEB
BLOCK TRANSMITTER
BLK
BLOCK RECEIVER
IBB/IEB
502
604
ERROR DETECTOR
602
ACK WAIT BLOCK MANAGEMENT SECTION
ACK
ACK TRANSMITTER
504
ERROR DETECTOR
603
503
RE-TRANSMISSION CONTROLLER
NACK
NACK TRANSMITTER
TRANSMITTING PARTY
RECEIVING PARTY

FIG. 8



BLOCK TRANSFER & RE-TRANSMISSION CONTROL (EXAMPLE 1)

FIG. 9



BLOCK TRANSFER & RE-TRANSMISSION CONTROL (EXAMPLE 2)

FIG. 10

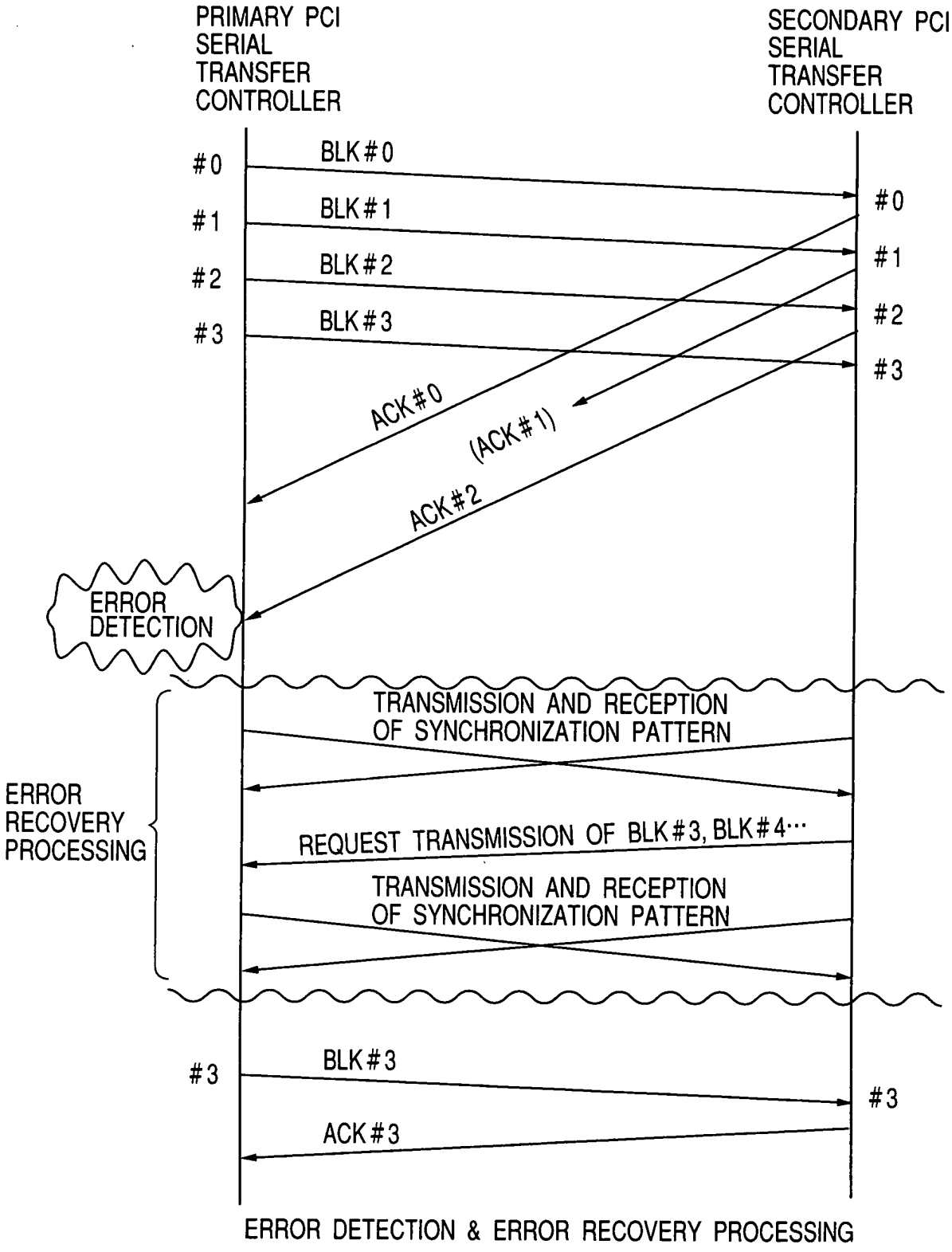

PRIMARY PCI SERIAL TRANSFER CONTROLLER
SECONDARY PCI SERIAL TRANSFER CONTROLLER
#0
BLK#0
#0
#1
BLK#1
#1
#2
BLK#2
#2
#3
BLK#3
#3
ACK#0
(ACK#1)
ACK#2
ERROR DETECTION
TRANSMISSION AND RECEPTION OF SYNCHRONIZATION PATTERN
ERROR RECOVERY PROCESSING
REQUEST TRANSMISSION OF BLK#3, BLK#4···
TRANSMISSION AND RECEPTION OF SYNCHRONIZATION PATTERN
#3
BLK#3
#3
ACK#3
ERROR DETECTION & ERROR RECOVERY PROCESSING

FIG. 11